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Nanomedicine and Nanoscience Research

Editorial

Li JV, et al. J Nanomed Nanosci: JNAN-102.
DOI: 10.29011/JNAN-102.100002

Admittance Spectroscopy Characterization of Some Electrical Properties in Nanomaterial-Based Diodes

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Citation: Li JV, Crandall RS, Repins IL, Nardes AM, Levi DH, et al. (2016) Admittance Spectroscopy Characterization of Some Electrical Properties in Nanomaterial-Based Diodes. J NanomedNanosci: JNAN-102. DOI: 10.29011/JNAN-102.100002

Received Date: 13 July, 2016; **Accepted Date:** 23 July, 2017; **Published Date:** 1 August, 2017

Abstract

We use admittance spectroscopy to extract some electrical properties of materials and devices consisting of nanostructures. The admittance spectroscopy technique has been traditionally used to extract the electrical properties ofdefects that act as majority-carrier traps. In semiconductor junction-based devices, especially where nanomaterials and nanostructures are present, a number ofpractical mechanisms may contribute to the admittance spectroscopy measurement and complicate its interpretation. Such complexities arise from the deviation of assumptions by the conventional admittance spectroscopy technique, i.e., the semiconductor being single-junction, consisting of ohmic contact, and measuringmostly in reverse bias. This work presents experimental investigation to identify the origins of some admittance spectroscopy signatures that are not due to majority-carrier traps, namely, dielectric relaxation, non-ohmic contact, and minority carrier inversion at hetero-interface.From these respective origins, we extend the admittance spectroscopy techniqueto effectivelyextractnon-majority-carrier trap properties: majority-carrier mobility, contact potential barrier, and minority-carrier inversion strength. These methods are applied to Cu(In,Ga)Se_2, Si hetero-junction diodes, and organic semiconductordevices based on nanomaterials.

Keywords: Admittance Spectroscopy; Back Contact Barrier; Carrier Freeze-Out; Carrier Type Inversion

Introduction

Defects are undoubtedly among the most critical physical issues to address for semiconductor materials, especially those containing nanomaterials and structures. Admittance spectroscopy, among other capacitance spectroscopy techniques such as capacitance-voltage carrier density profiling and deep-level transient spectroscopy, is commonly used to characterize majority-carrier trapping defects in Schottky or PN junction-based devices. Admittance spectroscopy measures the electrical response of a device to small AC bias voltage stimulation and its dependence on frequency and temperature, sometimesalso DC bias, presumably due to the capture and emission of the electrically active defects. It is possible to extractmajority-carrier trapping defect properties, i.e., their activation energy, capture cross-section, and density of states [1,2].

The nanotechnology research community depends on maintaining the certainty that the signals measured by admittance spectroscopy and interpreted as defects are truly due to majority-carrier traps. Without that, confusion may ensue. Unfortunately, only under certain simple circumstances can it be truly assumed that admittance spectroscopy reflects only majority-carrier trapping/de-trapping behaviors. Recent semiconductor junction-based devices are increasingly sophisticatedly with inclusion of constituent functional blocks such as Nano-structured materials, polycrystalline absorbers, heterojunctions, and non-ideal contacts. The complex nature of these practical devices means that other mechanismsmay also contribute to the admittance measurement. Therefore, one should be cautious not to always attribute without discretion all admittance spectroscopy measurements to majority-carrier trapping defects. An overview of such mechanisms is theoreticallydescribed in [3] usingsimulations.The first motivation of this work is to describeexperimentally observation “Defect Signatures” that are actual not majority-carrier trapping defects and devise guidelines to identify the actual physical origins.

The second motivation of this work is to take advantage of the so-called “Interferences” for conventional admittance spectroscopy and instead extract usefulinformation regarding the materials and devices: majority-carrier mobility, non-ohmic contact potential

barrier, and minority-carrier inversion at certain heterojunction. All these properties are characterized in a finished device environment (i.e., after the device fabrication is completed) rather in unfinished materials such as at the intermediate stage of wafer or thin-film level. Such properties are usually important to device operation and could be difficult to characterize by other techniques, which may be only applicable at unfinished material stage. Therefore, one mayrealize unique opportunities of extracting these non-majority-trap-related properties from non-conventional application of the admittance spectroscopy technique. We develop characterization methods and apply them to various semiconductor junction-based devices: CdTe, Cu(In,Ga)Se_2 (CIGS), silicon heterojunction solar cells with an intrinsic thin (HIT) amorphous silicon layer, and poly(3-hexylthiophene) organic semiconductor material. The junction-based devices used in this work were designed and optimized for solar cell applications and all contain nanostructured materials. Note that the methodology and interpretation need not be limited to solar cells but can be readily extended to other junction-based devices such as photodetectors and light-emitting diodes.

Experiment

Experiment Setup

We conducted admittance spectroscopy measurements using a Keysight 4294A impedance analyzer. The AC modulation voltage was 35 mV_{rms} unless otherwise specified. A Lakeshore 331A temperature controller was used to stabilize and measure the cold-finger temperature (ranging from 14 to 400 K) in a closed-loop helium cryostat. For more accurate measurement of sample temperature, we recorded the sample temperature from a temperature sensor attached directly to the top side, i.e., sample side and the electrical contact side, of the substrate. The other side, i.e., the bottom side, is in contact with the copper stage of the cold finger. At each fixed temperature, we applied a series of DC bias voltages to the device. A logarithmic frequency sweep was carried out at each DC bias voltage. For corroborative experiments, we also conducted the DC current density voltage (JV) measurements at each temperature using an HP 4140 semiconductor parameter analyzer.

Samples

The fabrication process of CdS/CdTe thin-film diode devices was similar to previous report [4] with the addition that gold is also experimented with as the back-contact metal. The CdS/Cu(In,Ga)Se_2 thin-film diode device was fabricated using the standard process [5], except that the growth temperature for the Cu(In,Ga)Se_2 film in this study was 435^{0}C. This growth temperature was selected to produce low carrier density in the absorber so that its dielectric relaxation frequency is below 100 MHz.In both the CdS/CdTe samples, the CdS layer was deposited using chemical-bath deposition that lead to nanostructures containing domains on order of 10-50 nm in size. The Si heterojunction cells with an intrinsic thin layer were grown on n-type wafers. The samples were taken from a previously reported sample set, the fabrication details of which were reported elsewhere[6]. The nominally amorphous silicon layer may contain nanostructures and indeed may intentionally incorporate nanostructures for performance considerations. The Poly(3-hexylthiophene) (P3HT) polymer sample was fabricated by spin coating P3HT from solution onto a Poly(3,4-ethylenedioxythiophene) Poly (styrene- sulfonate) (PEDOT:PSS) layer on top of indium tin oxide-coated glass, which results in Nano-scale structures typical of such organic materials. The other contact is aluminum. The fabrication process of the GaAsN diodes was similar to previous report [7].

Results

Assumptions and Violations

(Figure 1) illustrates the principle of the conventional treatment of admittance spectroscopy in the case of a single majority-carrier trapping defect.

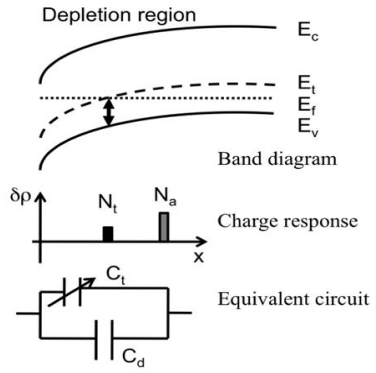

Figure 1: Band Diagram, Charge Response, And Equivalent Circuit of Conventional Admittance Spectroscopy Study: The Case of a Majority Carrier Trapping Defect Characterized by Energy EtAnd Uniform Density Nt With a Back Ground Free Carrier Density of Na.

The charge response due to the defect contributes to the total measured capacitance (in this work we limit our discussion to capacitance, i.e., the imaginary part of the admittance, while keeping in mind that similar discussion also applies to conductance).

The equivalent circuit of this physical system comprises of two capacitors in parallel: the depletion capacitance Cd due to the free carriers and Ct due to the majority-carrier trapping defect. The temperature-frequency dependence of Ct is governed by the thermal activated capture-emission rate of those defects whose energy Et intercepts the Fermi level Ef. It is from this temperature-frequency dependence (example of data taken from a GaAsN solar cell is shown in (Figure 2).

That the defect parameters such as activation energy, capture cross-section, and density of states are extracted[1,2,8].Application of admittance spectroscopy to majority-carrier trapping defect in the absorber of a typical solar cell device usually assumes that several conditions are satisfied: 1) the absorber is conductive enough and the dielectric relaxation frequency of bulk absorber material is out of (higher than) the range of measurement frequency; 2) only one junction is present and both contacts are ohmic; 3)

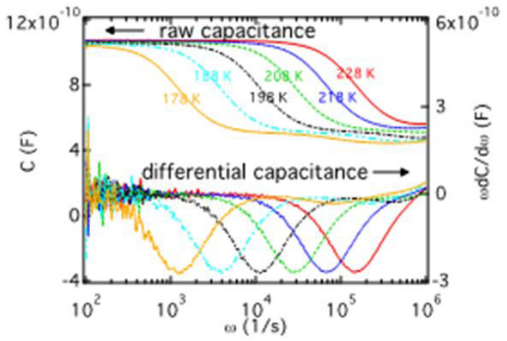

Figure 2: Frequency Dependent Raw (Top) And Differential (Bottom) Capacitance Spectra Taken from A Gaasn Solar Cell at Various Temperatures.

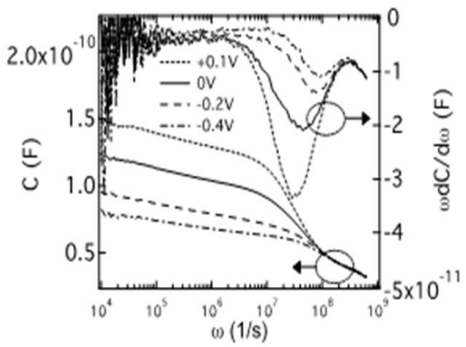

Figure 3: Bias Dependence of the Raw (Solid) and Differential (Dashed) Capacitance Spectra (Plotted Against Frequency) of aCIGS Solar Cell Measured at Room Temperature. The Bias Dependence of the Frequency Dispersion Characteristics is Due tothe Majority Carrier Freeze-Out.

only majority-carrier traps are observed; and 4) the junction is in reverse bias. With these simplifications, it is safe to consider that admittance spectroscopy reflects the behavior of majority-carrier trapping defects. However, the complex nature of most practical PV devices means that one or more of these conditions may often be violated in the admittance measurement. As a result, one or more circuit elements may be added (either in series with or in parallel to C_d) in the equivalent circuit in (Figure 1). The following is list possible mechanisms of violation:

1. Majority carrier freeze-out
2. Non-ohmic back contact
3. Free carrier's due to inversion

Majority Carrier Freeze-Out

If the free carrier density and mobility of the absorber are not high enougha probable situation due to either low free carrier density or low mobility the first condition about dielectric relaxation may not be met. The dielectric relaxation of a bulk semiconductor is given by $\omega_{dr}=1/\rho\varepsilon$, where $\rho$is the resistivity and $\varepsilon$is the permittivity.

In the case of high absorber resistivity or low measurement temperature, the dielectric relaxation frequency may fall into the range of interest. The hallmark of majority carrier freeze-out phenomenon is that: at a temperature lower (or frequency higher) than the transition point, the capacitance approaches the geometrical capacitance value.When dielectric relaxation cannot be neglected, the equivalent circuit of the quasi-neutral absorber (Figure3) is modeled as a parallel connection of capacitance C_b and resistance G_b.

The quasi-neutral absorber electrically behaves as G_b below the dielectric relaxation frequency and C_b above.In the presence of the junction depletion capacitance, the dielectric relaxation frequency of the absorber is modified [9] by a factor of W/t, where W is the depletion width and t is the absorber thickness. Because W varies with bias voltage, the modified dielectric relaxation frequency becomes bias dependent. We developed a method to measure mobility from the bias dependence of the dielectric relaxation frequency (example taken from a CIGS cell is shown in (Figure 4)[10].

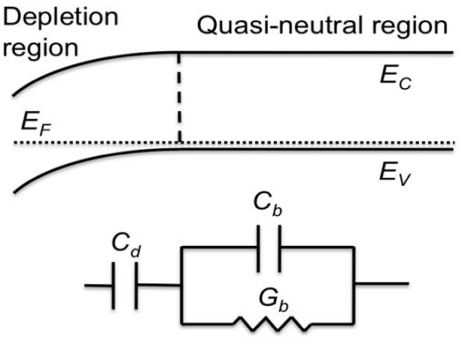

Figure 4: Band Diagram and Equivalent Circuit of a Solar Cell with a Depletion Region and a Quasi-Neutral Absorber Connected in Series.

The hole mobility (T = 300 K) of the CIGS device measured is 0.66 $cm^2/V/s$. This method works well on other low-mobility devices such as P3HT (where we measured a mobility $10^{-6\sim-4}$ $cm^2/V/s$ consistent with measurements using other techniques [11], CdTe (at low temperature) [10], and a-Si. Incidentally, the extracted activation energy of carrier freeze-out is due to the temperature dependence of both the carrier density and mobility.

Back Contact Potential Barrier

It is also possible to violate the second condition, which demands that only one junction is present in the device. In that case, the non-ohmic back contact contributes additional capacitive represented by C_c in (Figure 5) and conductive C_c in (Figure5) components to the equivalent circuit.

CdTe thin-film devices are prime candidates because of the difficulty of forming a high-quality, ohmic back contact. Peak 2 in (Figure6) is actually due to the back-contact barrier, while Peak 1 and 3 are due to majority carrier freeze-out and Cu-related defects, respectively [12].

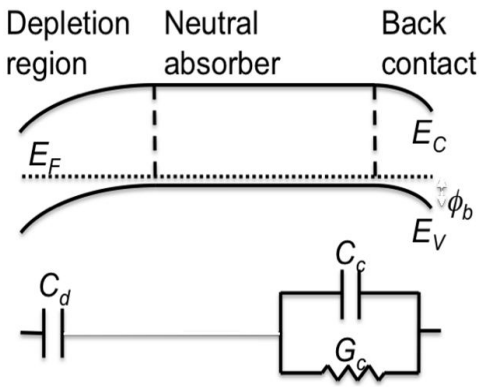

Figure 5: The Band Diagram and Equivalent Circuit Illustrating the Contribution to Admittance Measurements by a Non-Ohmic Back-Contact.

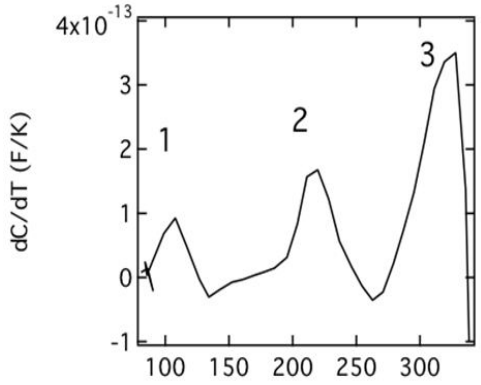

Figure 6: The Temperature Differential Capacitance Measured at 43.7 Khz From aCdTe Solar Cell.

The activation energy extracted from peak 2 consistently agrees with that from the rollover feature seen in temperature dependent JV curves (data not shown), which has been identified as attributable to the back-contact barrier[12-14]. For example, the CdTe device with a gold contact yielded a back-contact barrier height of 422 ± 5 meV from admittance spectroscopy and 424 ± 20 meV from the temperature dependent dark JV experiment. In contrast, the back-contact barrier height for devices with graphite contacts is 494 ± 9 meV from admittance spectroscopy and 552 ± 10 from the temperature dependent dark JVexperiment. The temperature dependent dark JV experiment serves as a useful correlated experiment to identify the secondary potential barrier. Observation of back contact potential in CIGS material has been reported [13]. In principle, this method applies to any PV devices where the back-contact scheme has not been optimized. We have seen successful applications (data not shown here) to novel PV device technology such as $Cu_2(Zn,Sn)Se_4$, OPV, and quantum dots.

Carrier Type Inversion

Under most circumstances, admittance spectroscopy measures contributions from the response of majority carriers. There are usually not enough minority carriers to have a significant capacitance contribution. In certain devices with highly asymmetrical doping, especially with the presence of a suitable heterointerface, it is possible for inversion to occur in a region where the minority-carrier density is significant. The CdS/CIGS heterointerface is such an example [15]. The inversion layer reduces interface recombination by repelling the majority carriers. The charge response due to the presence of free (and inverted) carriers reflects itself as a capacitance Ci in parallel with the depletion capacitor C_d(Figure. 7).

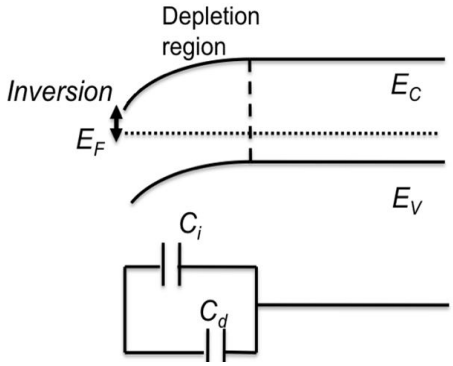

Figure 7: Band Diagram of an N-Type HIT Cell Showing the Inverted Region at the A-Si/C-Si Interface.

The temperature-frequency dependence of Ci is determined by the thermal activated nature of charge exchange between the Fermi level and the inversion layer.Recently, there has also been an increasing interest in understanding the inversion phenomenon at the amorphous (a-Si) and crystalline (c-Si) interface in a HIT cell. We show in (Figure 7) the band diagram of a HIT cell fabricated on n-type substrate. An activation energy of 0.14-0.28 eV is observed in these devices. There is no known bulk defect of this energy in the crystalline silicon. After further ruling out the valence-band offset (~0.45 eV), we conclude that this activation energy is the measurement Fermi level at the a-Si/c-Si interface. The band bending is large enough at the interface such that that region is strongly inverted. The exchange of holes whose density is comparable with that of electrons in the bulk, between the valence band and the Fermi level can thus significantly contribute to an observable admittance spectroscopy signal. Corroborative experiments such as DLTS and bias/illumination dependent admittance spectroscopy are helpful in providing additional information on the behavior of the inversion layer. We note that the above interpretation can also be proven by calculating the band bending from measured carrier density and built-in voltage. Application of this method has been reported in CIGS devices [15] and more recently in n-type Si HIT cells [16].

Conclusion

In conclusion, we show that many physical mechanisms oth-

er than majority-carrier trapping defects contribute to admittance spectroscopy measurements. These contributions occur because the breakdown of certain assumptions of conventional admittance spectroscopy, namely: single junction, ideal contacts, majority carrier only, and measurement in reverse bias. This work first identifies the possible physical origins of "Interference" and distinguishes them from the real defect signatures. More importantly, we take advantage of such "Interference" and devise methods to extract important material and device characteristics using admittance spectroscopy. We study several non-majority-trap-related properties that are commonly seen in admittance spectroscopy measurement of semiconductor junction-based devices: majority-carrier mobility, freeze-out of majority-carrier density or mobility, contact potential barrier height, and density of inverted minority carriers. The list of properties possible to extract by admittance spectroscopy, including both the conventional method and the new development reported in this work, is summarized in (Figure8).

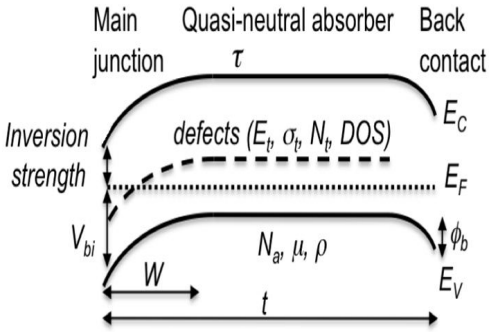

Figure 8: Parameters Possible to Be Extracted by Admittance Spectroscopy. The Conventional Method (In Combination with Capacitance-Voltage Technique) Can Be Used to Extract N_a, W, V_{bi}, E_t, σ_T, N_t, And DOS of Defects. The Methods Described in This Work Can Be Used to Extract μ, ρ, T, φ_B, E_F At the Interface, And Minority Carrier Lifetime τ. The Symbols Are Defined in The Text.

Such properties are usually important to semiconductor device operation and could be difficult to characterize by other techniques. The validity and applicability of these methods are demonstrated by application to a variety of semiconductor junction-based devices containing Nano-structured materials: CdTe, Cu(In,Ga)Se_2, silicon heterojunction cells with an Intrinsic Thin (HIT) amorphous silicon layer, and poly(3-hexylthiophene) organic semiconductor devices

Acknowledgment

This work was supported in part by the U.S. Department of Energy Under Contract No. DE-AC-36-08-GO28308.

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